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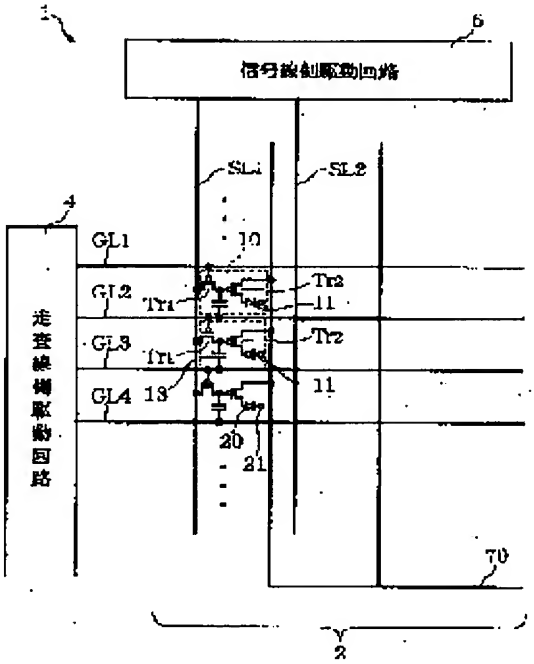
## (54) EL DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an EL(electroluminescence) display device in which an after image is suppressed and a clear image can be recognized without reducing the aperture ratio of pixels.
SOLUTION: An EL display device 1 has a display section 2, in which unit pixels 10 are arranged in a matrix manner, a signal line side drive circuit 6 and a scanning line side drive circuit 4. Each unit pixel 10 has an EL element 11, a switching transistor Tr1, a driving transistor Tr2 and an auxiliary capacitor 13. One electrode of the auxiliary capacitor 13 is connected to a gate electrode of the transistor Tr2 and the other electrode of the capacitor 13 is connected to a succeeding-stage scanning line GL. The scannning line drive circuit 4 outputs a blanking signal to forcibly stop the light emitting condition of the elements 11 via the succeeding-stage scanning line GL during a holding period during which the voltages written in the gate electrode of the transistors Tr2 is held. Thus, a blanking period in which the elements are not light emitting is inserted within one frame.

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* NOTICES *



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2.**** shows the word which can not be translated.
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CLAIMS

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[Claim(s)]
[Claim 1] While having two or more scanning lines with which a scan signal is supplied, and two or more signal lines with which a picture signal is supplied, a unit pixel is arranged in the shape of a matrix. Each unit pixel An EL element and the transistor for a drive which controls the amount of currents supplied to said EL element through a current supply source line, The display which comes to have the transistor for switching which changes a flow and cutoff with said signal line and the gate electrode of said transistor for a drive by change of switching operation while switching operation changes with scan signals, While supplying a scan signal to the signal-line side drive circuit which supplies a picture signal to said signal line, and said scanning line EL display characterized by having the scanning-line side drive circuit which outputs the blanking signal for stopping the luminescence condition of said EL element compulsorily through the scanning line within the maintenance period holding the electrical potential difference written in the gate electrode of said transistor for a drive.
[Claim 2] Said blanking signal is an EL display according to claim 1 which is the signal which sets said transistor for a drive as an OFF condition compulsorily.
[Claim 3] It is EL display according to claim 2 with which said unit pixel is equipped with the auxiliary capacity by which one electrode was connected to the gate electrode of said transistor for a drive, and the electrode of another side was connected to any one specific scanning line in said two or more scanning lines, and said blanking signal is given to the gate electrode of the transistor for a drive through said auxiliary capacity from said specific scanning line.
[Claim 4] EL display according to claim 3 said whose specific scanning line is the latter scanning line to the scanning line connected to the pixel chosen.
[Claim 5] Both said transistor for switching and said transistor for a drive are EL display according to claim 4 with which it is a P channel mold transistor, the anode electrode of said EL element was constituted as a pixel electrode, and the cathode electrode of said EL element was constituted as a counterelectrode.
[Claim 6] Both said transistor for switching and said transistor for a drive are EL display according to claim 4 with which it is an N channel mold transistor, the cathode electrode of said EL element was constituted as a pixel electrode, and the anode electrode of said EL element was constituted as a counterelectrode.
[Claim 7] Said transistor for switching is an EL display according to claim 4 which is the transistor which has the multi-gate structure where two or more transistors were connected to the serial.
[Claim 8] Said transistor for switching is an EL display according to claim 4 which is the transistor which has LDD (Lightly dopeddrain) structure.
[Claim 9] Said sub-picture element is equipped with a sub-picture element electrode, the transistor for switching, the transistor for control, auxiliary capacity, and the scanning line according to an individual, respectively, by dividing said each unit pixel into two or more sub-picture elements, while gradation is displayed by combining ON/OFF of each of said sub-picture element, a blanking signal is given through the scanning line for every sub-picture element, and it is EL display according to claim 4.
[Claim 10] EL display according to claim 9 with which weighting of the area for a light-emitting part of the EL element in said sub-picture element is carried out corresponding to the number of bits inputted according to the gradation to display.
[Claim 11] EL display according to claim 4 with which said transistor for switching and said transistor for a drive are formed by polish recon.
[Claim 12] EL display according to claim 4 whose active region of said transistor for a drive is a linear field.
[Claim 13] Any one specific scanning line in said two or more scanning lines is connected with the anode electrode of said EL element through said transistor for control. It was constituted as a counterelectrode and, as for the cathode electrode of said EL element, said specific scanning line serves as said current supply source line. While the luminescence drive of said EL element is carried out by the current which flows towards said EL element from said specific scanning line and said blanking signal is supplied from said specific scanning line This blanking signal is an EL display according to claim 1 which is the signal set as the voltage level lower than the potential of the cathode electrode of an EL element.
[Claim 14] Any one specific scanning line in said two or more scanning lines is connected with the cathode electrode of said EL element through said transistor for control. It was constituted as a counterelectrode and, as for the anode electrode of said EL element, said specific scanning line serves as said current supply source line. While the luminescence drive of said EL element is carried out by the current which flows towards said specific scanning

line from said EL element and said blanking signal is supplied from said specific scanning line This blanking signal is an EL display according to claim 1 which is the signal set as the voltage level higher than the potential of the anode electrode of an EL element.
[Claim 15] EL display according to claim 13 said whose specific scanning line is the preceding paragraph scanning line.
[Claim 16] EL display according to claim 13 whose sum of the output impedance of the last stage buffer in the scanning-line side drive circuit connected to the impedance of said specific scanning line and said specific scanning line is 20% or less to the impedance of the EL element connected to said specific scanning line.
[Claim 17] Said sub-picture element is equipped with a sub-picture element electrode, the transistor for switching, the transistor for control, auxiliary capacity, and the scanning line according to an individual, respectively, by dividing said each unit pixel into two or more sub-picture elements, while gradation is displayed by combining ON/OFF of each of said sub-picture element, a blanking signal is given through the scanning line for every sub-picture element, and it is EL display according to claim 13.
[Claim 18] EL display according to claim 17 with which weighting of the area for a light-emitting part of the EL element in said sub-picture element is carried out corresponding to the number of bits inputted according to the gradation to display.
[Claim 19] While having two or more scanning lines with which a scan signal is supplied, and two or more signal lines with which a picture signal is supplied, a unit pixel is arranged in the shape of a matrix. Each unit pixel An EL element and the transistor for a drive which controls the amount of currents which flows to an EL element, In EL display which comes to have the transistor for switching which changes a flow and cutoff with said signal line and the gate electrode of said transistor for a drive by change of switching operation while switching operation changes with scan signals Wiring for blanking signals with which the blanking signal for setting said transistor for a drive as an OFF condition compulsorily within the maintenance period holding the electrical potential difference which was prepared for every line of the unit pixel arranged in the shape of [ said ] a matrix, and was written in the gate electrode of said transistor for a drive is supplied, The blanking signal drive circuit which supplies a blanking signal from said wiring for blanking signals, The auxiliary capacity by which it was prepared for said every unit pixel, one electrode was connected to the gate electrode of said transistor for a drive, and the electrode of another side was connected to said wiring for blanking signals, A preparation and said blanking signal are an EL display characterized by giving the gate electrode of the transistor for a drive through said auxiliary capacity from wiring for blanking signals.
[Claim 20] Said wiring for blanking signals is an EL display according to claim 19 connected according to the individual in said blanking signal drive circuit.
[Claim 21] Said wiring for blanking signals is an EL display according to claim 19 connected to said blanking signal drive circuit through one common Rhine.

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[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to EL (electroluminescence) display.
[0002]
[Description of the Prior Art] The configuration of the unit pixel of the conventional EL display is shown in drawing 32 and drawing 33 . In drawing 32 and drawing 33 , GL is [ auxiliary capacity and SL of the scanning line and 13 ] current supply source lines for a switching transistor and Tr2 to supply the transistor for a drive to EL element 11, and for an EL element and Tr1 supply a current in a signal line and 11, as for 70. If both the scanning line GL and the signal line SL are first turned on on the occasion of luminescence of EL element 11, a charge will be accumulated in the auxiliary capacity 13 through the transistor Tr1 for switching. And a luminescence drive is carried out by the current according to a current picture signal until a current continues flowing from the current supply source line 70 to EL element 11 and a picture signal is written in with the following frame, even if the transistor Tr1 for switching is turned off in order that this auxiliary capacity 13 may continue applying an electrical potential difference to the gate of the transistor Tr2 for a drive. By the way, in the above-mentioned conventional example, an EL element is continuing emitting light during an one-frame period. Therefore, if a movie display is performed, for an after-image phenomenon, the image of a frame will lap with the image of the following frame last time, and an image observer will recognize it as the image having faded. (2001 FPD technology encyclopedia p122) . As a remedy in such a case, if a blanking period (the period when luminescence of an EL element is stopped at and the whole screen will be in a black display condition is meant.) is inserted during the image display period of one frame, an after-image is controlled and it is known that an image will become clear. Based on such a view, the exclusive transistor for giving a blanking signal is prepared in JP,2000-221942,A, and the configuration which sets a blanking signal to ON at a predetermined period just before the next one-frame period starts is indicated.
[0003]
[Problem(s) to be Solved by the Invention] However, it is necessary to form an exclusive transistor and the control line which gives a blanking signal for every pixel with the above-mentioned configuration. Therefore, only an exclusive transistor and the occupancy surface integral of the control line cause decline in the numerical aperture of a pixel. Moreover, since an exclusive transistor and the control line are formed separately, the fall of the yield of a panel is caused.
[0004] The purpose of this invention is offering EL ********** which controls an after-image and enabled it to recognize a clear image, without solving the above-mentioned technical problem and causing decline in the numerical aperture of a pixel.
[0005]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, among this inventions invention according to claim 1 While having two or more scanning lines with which a scan signal is supplied, and two or more signal lines with which a picture signal is supplied, a unit pixel is arranged in the shape of a matrix. Each unit pixel An EL element and the transistor for a drive which controls the amount of currents supplied to said EL element through a current supply source line, The display which comes to have the transistor for switching which changes a flow and cutoff with said signal line and the gate electrode of said transistor for a drive by change of switching operation while switching operation changes with scan signals, While supplying a scan signal to the signal-line side drive circuit which supplies a picture signal to said signal line, and said scanning line It is characterized by having the scanning-line side drive circuit which outputs the blanking signal for stopping the luminescence condition of said EL element compulsorily through the scanning line within the maintenance period holding the electrical potential difference written in the gate electrode of said transistor for a drive.
[0006] While the image which the EL element of each pixel emits light according to a picture signal, and wishes to have by the above-mentioned configuration is displayed, the blanking period when an EL element does not emit light will be inserted into one frame. Therefore, in a movie display, a black display is inserted between the images of a frame last time the image of a frame, and next time. Consequently, an after-image phenomenon can be controlled and a clear image can be recognized now.
[0007] Moreover, the transistor of dedication for a blanking and wiring for blanking signals become unnecessary by supplying a blanking signal through the scanning line. Therefore, the numerical aperture of the part improves.
[0008] In addition, a condition with the vocabulary "a halt" near the drop dead halt else [ in case a luminescence condition stops completely ] is also included.

[0009] Moreover, invention according to claim 2 is EL indicating equipment according to claim 1, and said blanking signal is characterized by being the signal which sets said transistor for a drive as an OFF condition compulsorily. Here, the condition (very weak ON condition) near a perfect OFF condition is included besides in the case of a perfect OFF condition with the vocabulary "an OFF condition."
[0010] Moreover, invention according to claim 3 is EL indicating equipment according to claim 2, and said unit pixel is equipped with the auxiliary capacity by which one electrode was connected to the gate electrode of said transistor for a drive, and the electrode of another side was connected to any one specific scanning line in said two or more scanning lines, and it is characterized by giving said blanking signal to the gate electrode of the transistor for a drive through said auxiliary capacity from said specific scanning line.
[0011] Moreover, invention according to claim 4 is EL display according to claim 3, and said specific scanning line is characterized by being the latter scanning line to the scanning line connected to the pixel chosen.
[0012] for example, the own scanning line of a selection pixel -- **** for the specific scanning lines -- things are also possible. However, in this case, with the transition to the OFF from ON of a selection pulse, it is the effect of the parasitic capacitance of the transistor for a drive connected to the own scanning line of a pixel, it is expected that the potential of a pixel electrode changes, and in order to prevent this, it is necessary to add big storage capacitance. This problem is solvable by making the specific scanning line into the latter scanning line about this point. Moreover, leading about of wiring can be made into min by making the specific scanning line into the latter scanning line.
[0013] Moreover, invention according to claim 5 is EL indicating equipment according to claim 4, and both said transistor for switching and said transistor for a drive are P channel mold transistors, and it is characterized by having constituted the anode electrode of said EL element as a pixel electrode, and constituting the cathode electrode of said EL element as a counterelectrode.
[0014] By the above-mentioned configuration, driver voltage of the whole display can be made small compared with the case where the transistor from which a polarity differs is used.
[0015] Moreover, invention according to claim 6 is EL indicating equipment according to claim 4, and both said transistor for switching and said transistor for a drive are N channel mold transistors, and it is characterized by having constituted the cathode electrode of said EL element as a pixel electrode, and constituting the anode electrode of said EL element as a counterelectrode.
[0016] Also by the above-mentioned configuration, driver voltage of the whole display can be made small compared with the case where the transistor from which a polarity differs is used.
[0017] Moreover, invention according to claim 7 is EL indicating equipment according to claim 4, and said transistor for switching is characterized by being the transistor which has the multi-gate structure where two or more transistors were connected to the serial.
[0018] about the transistor for switching, there is little leakage current as the property demanded -- in other words, what has the good maintenance property of data is desired. Then, a good OFF property can be acquired by making the transistor for switching into multi-gate structure like the above.
[0019] Moreover, invention according to claim 8 is EL indicating equipment according to claim 4, and said transistor for switching is characterized by being the transistor which has LDD (Lightly doped drain) structure.
[0020] By the above-mentioned configuration, a good OFF property can be acquired like invention of the claim 7 above-mentioned publication.
[0021] Moreover, invention according to claim 9 is EL display according to claim 4, said each unit pixel is divided into two or more sub-picture elements, a blanking signal is given through the scanning line for every sub-picture element, and it is characterized [ said sub-picture element is equipped with a sub-picture element electrode, the transistor for switching, the transistor for control, auxiliary capacity, and the scanning line according to an individual, respectively and ] by things while gradation is displayed by combining ON/OFF of each of said sub-picture element.
[0022] EL display excellent in gradation nature is constituted by the above-mentioned configuration.
[0023] Moreover, invention according to claim 10 is EL display according to claim 9, and is characterized by carrying out weighting of the area for a light-emitting part of the EL element in said sub-picture element corresponding to the number of bits inputted according to the gradation to display.
[0024] The surface ratio for a light-emitting part of each sub-picture element which constitutes one unit pixel is corresponded to a bit, and it is 1:2:4. : -- It becomes possible by carrying out weighting to :2 (n-1) to display 2n gradation.
[0025] Moreover, invention according to claim 11 is EL indicating equipment according to claim 4, and is characterized by forming said transistor for switching, and said transistor for a drive by polish recon.
[0026] Polish recon has large mobility as compared with an amorphous silicon, and detailed-izing of a component is easy for it. Therefore, it is effective especially when using two or more transistors into 1 pixel like this invention.
[0027] Moreover, invention according to claim 12 is EL indicating equipment according to claim 4, and is characterized by the active region of said transistor for a drive being a linear field.
[0028] Even if the electrical potential difference impressed to the threshold of the transistor for a drive or the gate of the transistor for a drive varies, it can avoid almost affecting a current value by operating the transistor for a drive in a linear field like the above. Therefore, at the former, it can be used also with a transistor with a bad property which has been considered that it cannot bear use.
[0029] Moreover, invention according to claim 13 is EL display according to claim 1. Any one specific scanning line in said two or more scanning lines is connected with the anode electrode of said EL element through said transistor

for control. It was constituted as a counterelectrode and, as for the cathode electrode of said EL element, said specific scanning line serves as said current supply source line. While the luminescence drive of said EL element is carried out by the current which flows towards said EL element from said specific scanning line and said blanking signal is supplied from said specific scanning line It is characterized by this blanking signal being a signal set as the voltage level lower than the potential of the cathode electrode of an EL element.
[0030] Like the above, the current supply source line of the dedication for supplying a current to an EL element becomes unnecessary by supplying a current to an EL element from the specific scanning line. Consequently, while being able to make a numerical aperture larger than the conventional example, generating of the line defect short depended in the short-circuit between layers resulting from a current supply source line and a layer can be prevented, and EL display whose yield improved can be constituted.
[0031] Moreover, invention according to claim 14 is EL display according to claim 1. Any one specific scanning line in said two or more scanning lines is connected with the cathode electrode of said EL element through said transistor for control. It was constituted as a counterelectrode and, as for the anode electrode of said EL element, said specific scanning line serves as said current supply source line. While the luminescence drive of said EL element is carried out by the current which flows towards said specific scanning line from said said EL element and said blanking signal is supplied from said specific scanning line It is characterized by this blanking signal being a signal set as the voltage level higher than the potential of the anode electrode of an EL element.
[0032] The same operation as invention according to claim 13 is done so also by the above-mentioned configuration.

[0033] Moreover, invention according to claim 15 is EL display according to claim 13, and is characterized by said specific scanning line being the preceding paragraph scanning line.
[0034] Change of the pixel electrode potential resulting from the parasitic capacitance of a transistor can be controlled like the operation in invention of the claim 4 above-mentioned publication, without adding big storage capacitance.
[0035] Moreover, invention according to claim 16 is EL display according to claim 13, and the sum of the output impedance of the last stage buffer in the scanning-line side drive circuit connected to the impedance of said specific scanning line and said specific scanning line is characterized by being 20% or less to the impedance of the EL element connected to said specific scanning line. An impedance is regulated because the potential of the last train edge of the scanning line will fall, sufficient electrical potential difference for an EL element will no longer be impressed and a uniform display will not be obtained, if it exceeds 20%.
[0036] Moreover, invention according to claim 17 is EL display according to claim 13, said each unit pixel is divided into two or more sub-picture elements, a blanking signal is given through the scanning line for every sub-picture element, and it is characterized [ said sub-picture element is equipped with a sub-picture element electrode, the transistor for switching, the transistor for control, auxiliary capacity, and the scanning line according to an individual, respectively and ] by things while gradation is displayed by combining ON/OFF of each of said sub-picture element.
[0037] EL display excellent in gradation nature is constituted by the above-mentioned configuration.
[0038] Moreover, invention according to claim 18 is EL display according to claim 17, and is characterized by carrying out weighting of the area for a light-emitting part of the EL element in said sub-picture element corresponding to the number of bits inputted according to the gradation to display.
[0039] The surface ratio for a light-emitting part of each sub-picture element which constitutes one unit pixel is corresponded to a bit, and it is 1:2:4. : -- It becomes possible by carrying out weighting to :2 (n-1) to display 2n gradation.
[0040] While invention according to claim 19 is equipped with two or more scanning lines with which a scan signal is supplied, and two or more signal lines with which a picture signal is supplied, a unit pixel is arranged in the shape of a matrix. Moreover, each unit pixel An EL element and the transistor for a drive which controls the amount of currents which flows to an EL element, In EL display which comes to have the transistor for switching which changes a flow and cutoff with said signal line and the gate electrode of said transistor for a drive by change of switching operation while switching operation changes with scan signals Wiring for blanking signals with which the blanking signal for setting said transistor for a drive as an OFF condition compulsorily within the maintenance period holding the electrical potential difference which was prepared for every line of the unit pixel arranged in the shape of [ said ] a matrix, and was written in the gate electrode of said transistor for a drive is supplied, The blanking signal drive circuit which supplies a blanking signal from said wiring for blanking signals, The auxiliary capacity by which it was prepared for said every unit pixel, one electrode was connected to the gate electrode of said transistor for a drive, and the electrode of another side was connected to said wiring for blanking signals, A preparation and said blanking signal are characterized by giving the gate electrode of the transistor for a drive through said auxiliary capacity from wiring for blanking signals.
[0041] It is not necessary to prepare the transistor of dedication for a blanking, therefore the numerical aperture of the part improves by the above-mentioned configuration.
[0042] Moreover, invention according to claim 20 is EL indicating equipment according to claim 19, and said wiring for blanking signals is characterized by connecting according to an individual in said blanking signal drive circuit.
[0043] A blanking signal is supplied to different timing for every wiring for blanking signals by the above-mentioned configuration.
[0044] Moreover, invention according to claim 21 is EL indicating equipment according to claim 19, and said wiring for blanking signals is characterized by connecting with said blanking signal drive circuit through one common Rhine.

[0045] A blanking signal is supplied from each wiring for blanking signals to the same timing by the above-mentioned configuration.
[0046]
[Embodiment of the Invention] (Gestalt 1 of operation) Drawing 1 is the circuit diagram showing the configuration of the active-matrix mold EL display concerning the gestalt 1 of operation. The display 2 by which, as for the active-matrix mold EL display 1, the unit pixel 10 has been arranged in the shape of a matrix, The scanning-line side drive circuit 4 which outputs a scan signal to each unit pixel 10 through the scanning lines GL1 and GL2 and -- (a reference mark GL shows when naming the scanning line generically), It has the signal-line side drive circuit 6 which outputs a picture signal to each unit pixel 10 through signal lines SL1 and SL2 and -- (a reference mark SL shows when naming a signal line generically), and the current supply source line 70 for supplying a current to each EL element 11.
[0047] The unit pixel 10 has EL element 11 which functions as an illuminant of a unit pixel, the transistor Tr1 for switching, the transistor Tr2 for a drive which controls the amount of drive currents to EL element 11, and the auxiliary capacity 13. One electrode of the auxiliary capacity 13 is connected to the latter-part scanning line GL as the specific scanning line, and the electrode of another side of the auxiliary capacity 13 is connected to the gate of the transistor Tr2 for a drive, and the drain of a switching transistor Tr1 in common. Transistors Tr1 and Tr2 are all thin film transistors (TFT) of like-pole nature, and are constituted from the gestalt 1 of this operation by the P channel mold transistor.
[0048] Drawing 2 is the block diagram showing the configuration of a scanning-line side drive circuit, and drawing 3 is the circuit diagram showing the configuration of a part of scanning-line side drive circuit. The scanning-line side drive circuit 4 has the scanning lines GL1 and GL2, the selector circuits A1 and A2 corresponding to --, and -- (when naming a selector circuit generically, a reference mark A shows). Three input signals V1, V2, and V3 with which voltage levels differ are inputted into this selector circuit A, respectively. Moreover, in selector circuit A, they are two select signals Sa and Sb (when reference marks Sa and Sb show when naming a select signal generically, and a select signal is shown according to an individual, a subscript is given to reference marks Sa and Sb.). For example, in the case of the select signal relevant to a selector circuit A1, reference marks Sa1 and Sb1 show. It is inputted. And it is chosen by the combination of the logical value of these select signals Sa and Sb any of three input signals V1, V2, and V3 they are, and it is constituted so that it may be outputted to the scanning line GL.
[0049] In addition, select signals Sa and Sb are generated by the external controller (not shown), and are supplied to the scanning-line side drive circuit 4.
[0050] The concrete configuration of a selector circuit A1 is shown in drawing 3 . That is, the selector circuit A1 consists of four inverters 3a, 3b, 3c, and 3d and the five transfer gates 5a, 5b, 5c, 5d, and 5e.
[0051] Subsequently, actuation of a selector circuit A1 is explained. For example, when both the select signals Sa1 and Sb1 are logic "0", V1 is chosen and it is outputted to the scanning line GL1. If circuit actuation is explained briefly, the transfer gates 5a and 5c are in ON condition as Sa1 is logic "0", and transfer gate 5b will be in an OFF condition. Therefore, V1 is inputted into transfer gate 5d, and V3 is inputted into transfer gate 5e. On the other hand, since Sb1 is logic "0", transfer gate 5d is in ON condition, and transfer gate 5e will be in an OFF condition. Therefore, the inside V1 of V1 and V3 will be chosen, and it will be outputted to the scanning line GL1.
[0052] Based on the same actuation as the above, when a select signal Sa1 is logic "0" and a select signal Sb1 is logic "1", V2 is chosen and it is outputted to the scanning line GL1. When a select signal Sa1 is logic "1" and a select signal Sb1 is logic "0", V3 is chosen and it is outputted to the scanning line GL1.
[0053] Thus, a selector circuit A1 chooses any of V1-V3 they are according to the logical value of select signals Sa1 and Sb1, and outputs it to the scanning line GL. [ it ]
[0054] The selector circuit A2 of the remainders other than selector circuit A1 and -- have the same configuration as a selector circuit A1, choose any of V1-V3 they are according to the combination of the logical value of a select signal Sa2, Sb2;Sa3, and Sb3;-- like a selector circuit A1, and output it to the scanning lines GL2 and GL3 and --. [ it ]
[0055] In this way, the scanning-line side drive circuit 4 is constituted so that it may choose any of V1-V3 they are and may output to the scanning line GL.
[0056] In addition, with the gestalt 1 of this operation, V1 is set as the voltage level which turns ON the transistor Tr1 for switching, and V2 is set as the voltage level which turns OFF the transistor Tr1 for switching. That is, V1 and V2 are equivalent to the usual scan signal. Moreover, V3 is set as blanking signal-level level.
[0057] Drawing 4 is the sectional view showing a 1-pixel configuration, and drawing 5 is the top view showing a 1-pixel configuration. EL element 11 consists of EL luminous layers 22 arranged between the anode electrode 31 (it is equivalent to the pixel electrode 20 with the gestalt of this operation), the cathode electrode 32 (it is equivalent to a counterelectrode 21 with the gestalt of this operation), and the anode electrode 31 and the cathode electrode 32 as shown in drawing 4 . In addition, for 35, as for gate dielectric film and 38, in drawing 4 , a glass substrate and 37 are [ the flattening film and 39 ] interlayer insulation films.
[0058] Moreover, in drawing 4 , said anode electrodes 31 are transparent electrodes, such as indium TIN oxide (ITO), and the cathode electrode 32 is an opaque electrode (metal electrode which consists of these metals, such as Mg and aluminum, or an alloy with Ag, Li, etc.). Therefore, the light from the EL luminous layer 22 is irradiated from a glass substrate 35 side. In addition, EL element 11 may be the configuration of being an inorganic EL element and having a charge impregnation layer and a charge transportation layer also with an organic EL device. That is, not the thing limited to the thing of a configuration of being shown in drawing 4 but a well-known EL element can be used. In

addition, transparence substrates, such as resin films, such as not only glass but a polycarbonate, polymethylmethacrylate, polyethylene terephthalate, etc., may be used for a substrate 35 that what is necessary is just what can **** an EL element.

[0059] Subsequently, the display action of EL display of the above-mentioned configuration is explained. Drawing 6 is the timing chart of luminescence actuation of an EL element. Drawing 6 (a) is the wave form chart of a picture signal electrical potential difference, drawing 6 (b) is the wave form chart of the electrical potential difference of the scanning line GLa, and drawing 6 (c) is the wave form chart of the electrical potential difference of the scanning line GLb. Here, two pixels 10a and 10b of explanation which is shown in drawing 7 for convenience and which adjoins up and down will be made into an example, and will be explained. In addition, in drawing 7 , Subscript a is attached about the component relevant to pixel 10a (for example, the scanning line is a reference mark GLa and Tr1a etc. shows the transistor for switching), and Subscript b is attached about the component relevant to pixel 10b (for example, the scanning line is a reference mark GLb and Tr1b etc. shows the transistor for switching). In addition, with the gestalt 1 of this operation, counterelectrode potential shall be set as 7.4V and the potential of the current supply source line 70 shall be set as 12.4V. Moreover, a picture signal has the binary voltage level of 5V and 12.4V, in the case of 5V, a luminescence condition shall be shown, and, in the case of 12.4V, a nonluminescent condition shall be shown.

[0060] First, as shown in drawing 6 (b), in time of day T1, the scanning line GLa of this stage is changed from V2 level (the gestalt 1 of this operation 12.4 V) to V1 level (the gestalt 1 of this operation 0 V), and pixel 10a is chosen. Thereby, transistor Tr1a for switching which is a P channel mold transistor will be in ON condition. According to ON condition of this transistor Tr1a, a picture signal electrical potential difference (7.4V) is impressed to the gate of transistor Tr2a for a drive, and auxiliary capacity 13a through a signal line SL. That is, the period of T2 is equivalent to the write-in period of a picture signal from time of day T1. Here, since the potential of the current supply source line 70 is set as 12.4V, 7.4-12.4=-5V are impressed between the gate sources of transistor Tr2a for a drive. Thereby, transistor Tr2a for a drive is set to ON, a current flows towards a cathode electrode (counterelectrode) through the current supply source line 70 and transistor Tr2a for a drive from the anode electrode (pixel electrode) of EL element 11a, and EL element 11a emits light.

[0061] And the electrical potential difference written in the gate electrode of transistor Tr2a for a drive is held, and EL element 11a continues emitting light according to a predetermined drive current. In time-of-day T3 within the maintenance period when the electrical potential difference written in the gate electrode of this transistor Tr2a for a drive is held, a blanking signal is given to auxiliary capacity 13a through the latter-part scanning line GLb. That is, the latter scanning line GLb serves as the blanking signal level V3 (the gestalt of this operation 17.5 V) by time-of-day T3. Thereby, since capacity coupling of the gate electrode of transistor Tr2a for a drive is carried out to the latter scanning line GLb, about [ 5V ] potential increases the gate potential of transistor Tr2a for a drive. For this reason, the potential between the gate sources of transistor Tr2a for a drive is set to about 0, transistor Tr2a for a drive turns off, and luminescence of EL element 11a stops. In addition, the auxiliary capacity 13 shall be set as sufficiently big capacity value to the gate capacitance of the transistor Tr2 for a drive. It is because the gate potential of transistor Tr2a for a drive hardly changes and cannot turn off transistor Tr2a for a drive, even if a blanking signal will be supplied, if set up conversely.

[0062] Thus, in time-of-day T3 within the maintenance period when the electrical potential difference written in the gate electrode of transistor Tr2a for a drive is held, a blanking signal is outputted through the scanning line GLb, and, thereby, luminescence of EL element 11a stops compulsorily.

[0063] Although it was made for luminescence of an EL element to stop completely, you may make it become the extinction (for an intensity level to be less than about 1% of brightness) instead of quenching at which luminescence stopped with the blanking signal level given to the gate of transistor Tr2a in the above-mentioned example. Moreover, since an EL element has the high-speed responsibility of mus order, even if it is a blanking signal which is the pulse width (T3 - T four) of ms order, it can perform the blanking of an EL element.

[0064] Subsequently, if the scanning line GLa is chosen by time-of-day T four, a picture signal electrical potential difference will be written in like the above. Since, as for a picture signal electrical potential difference, 12.4V (signal level which shows a nonluminescent condition) are written in at this time, transistor Tr2a for a drive will be in an OFF condition, an EL element stops luminescence and a nonluminescent condition is held till the next frame period. The nonluminescent condition at this time is not based on a blanking signal based on image data. In this way, while the luminescence drive of the pixel 10a is carried out corresponding to a picture signal, a blanking condition is acquired within an one-frame period.

[0065] Although the above-mentioned example explained the luminescence actuation about pixel 10a, actuation with the same said of other pixels is performed, the EL element which is each pixel emits light according to a picture signal, and while the image to wish to have is displayed, the blanking period when an EL element does not emit light will be inserted into one frame. Therefore, in animation display, last time, a black display is inserted between the images of a frame, an after-image phenomenon can be controlled and, thereby, an image can be vividly recognized to be the image of a frame now next time.

[0066] In addition, although the transistor Tr2 for a drive can also use an N channel mold transistor, it is desirable to use a P channel mold transistor like the gestalt of this operation. It is because an electrical potential difference required for an electrical potential difference with the gate voltage higher than the anode of an EL element for making the transistor Tr2 for a drive into ON condition to be needed, and drive a active-matrix mold EL element will increase if the transistor Tr2 for a drive is formed with an N channel mold transistor.

[0067] (Gestalt 2 of operation) Drawing 8 is the sectional view showing the 1-pixel configuration of the active-matrix mold EL display concerning the gestalt 2 of operation. The gestalt 2 of this operation all uses transistors Tr1 and Tr2 as an N channel mold transistor, and uses the cathode electrode of an EL element as a pixel electrode, and is characterized by constituting an anode electrode as a counterelectrode, and the other configurations of it are the same as that of the gestalt 1 of the above-mentioned implementation. With the gestalt 2 of this operation, a cathode electrode is used as an opaque electrode and uses an anode electrode as an ITO electrode. With such a configuration, the light from a luminous layer will be irradiated from the opposite side in a substrate 35. Therefore, with the gestalt 2 of this operation, a substrate 35 does not necessarily need to use a transparence substrate like the gestalt 1 of operation, and may use opaque substrates, such as silicon.
[0068] Moreover, although the transistor Tr2 for a drive may be a P channel mold transistor when the cathode electrode of an EL element is used as a pixel electrode and it constitutes an anode electrode as a counterelectrode, it is more desirable to use an N channel mold transistor from a viewpoint of low-battery-izing. In addition, the display action of the active-matrix mold EL display concerning the gestalt 2 of this operation is the same as that of the gestalt 1 of the above-mentioned implementation, an EL element is made to emit light according to a picture signal, and a blanking period is inserted while displaying the image to wish to have.
[0069] Drawing 9 is the timing chart of luminescence actuation of EL indicating equipment concerning the gestalt 2 of operation. Drawing 9 (a) is the wave form chart of a picture signal electrical potential difference, drawing 9 (b) is the wave form chart of the electrical potential difference of the scanning line GLc, and drawing 9 (c) is the wave form chart of the electrical potential difference of the scanning line GLd. Here, two pixels 10c and 10d which are shown in drawing 10 and which adjoin up and down will be made into an example, and will be explained. In addition, in drawing 10 , Subscript c is attached about the component relevant to pixel 10c (for example, the scanning line is a reference mark GLc and Tr1c etc. shows the transistor for switching), and Subscript d is attached about the component relevant to 10d of pixels (for example, the scanning line is a reference mark GLd and Tr1d etc. shows the transistor for switching).
[0070] First, as shown in drawing 9 (b), in time of day T1, the scanning line GLc of this stage is changed from V2 level (the gestalt 2 of this operation 0 V) to V1 level (the gestalt 2 of this operation 12.5 V), and pixel 10c is chosen. Thereby, transistor Tr1c for switching which is an N channel mold transistor will be in ON condition. According to ON condition of this N channel mold transistor Tr1c, a picture signal electrical potential difference (5.0V) is impressed to the gate of transistor Tr2c for an N channel mold drive, and auxiliary capacity 13c through a signal line SL. In addition, with the gestalt 2 of this operation, the potential of the current supply source line 70 is -5.0V, and counterelectrode potential is set as 0V. Therefore, since about 5 V is impressed between the gate sources of transistor Tr2c for a drive, transistor Tr2c for a drive is set to ON. Thereby, a current flows towards a cathode electrode (pixel electrode) from an anode electrode (counterelectrode), and EL element 11c emits light. And this luminescence condition is held to the timing (time-of-day T3) from which the latter scanning line GLd serves as the blanking signal level V3 (the gestalt of this operation -5.0 V). And since the gate electrode of transistor Tr2c for a drive is connected with the latter scanning line GLd through auxiliary capacity 13c, it is time-of-day T3 and, as for the gate potential of transistor Tr2c for a drive, about [ 5V ] potential decreases. For this reason, the potential between the gate sources of drive transistor Tr2c is set to 0, and luminescence of EL element 11c stops. In addition, the auxiliary capacity 13 shall be set as sufficiently big capacity value to the gate capacitance of the transistor Tr2 for a drive. It is because the gate potential of transistor Tr2c for a drive hardly changes and cannot turn off transistor Tr2c for a drive, even if a blanking signal will be supplied, if set up conversely.
[0071] In the above-mentioned example, also although it explains and excels about luminescence and the blanking about EL element 11c, luminescence and a blanking are obtained by actuation with the same said of the EL element of others other than EL element 11c.
[0072] Thus, also in the gestalt 2 of this operation, a blanking period can be inserted into one frame like the gestalt 1 of operation, the effect of an after-image is lost, and a clear image can be recognized now.
[0073] In addition, when system-wide pressure-proofing is allowed, you may make it constitute a transistor Tr1 and a transistor Tr2 from a transistor from which a polarity differs in this invention.
[0074] (Gestalt 3 of operation) Drawing 11 is the top view of the display of the display concerning the gestalt 3 of operation, and drawing 12 is the circuit diagram. In addition, drawing 11 and drawing 12 show only the configuration about 1 pixel. The gestalt 3 of this operation divides one unit pixel into two or more fields, and is characterized by indicating by gradation with an area gradient method. Hereafter, a concrete configuration is explained with reference to drawing 11 and drawing 12 .
[0075] The unit pixel 10 has the structure divided into two or more fields (the gestalt 3 of this operation four). The configuration of the sub-picture element 50 which is this division field is the same as the configuration of the unit pixel 10 in the gestalt 1 of the above-mentioned implementation. That is, a sub-picture element 50 has the transistor Tr1 for switching, the transistor Tr2 for a drive, and the auxiliary capacity 13 while having the scanning line GL, respectively.
[0076] It realizes by combining luminescence/nonluminescent one of the divided sub-picture element field as the method of presentation of gradation. In addition, a digital picture signal is supplied to a signal line SL. As the concrete approach of a gradation display, weighting of the area for a light-emitting part of EL element 11 in the sub-picture element 50 divided into two or more fields is carried out corresponding to the bit. Thus, it does not divide into division into equal parts, but the surface ratio for a light-emitting part is corresponded to a bit, and it is 1:2:4. : -- It becomes possible by carrying out weighting to :2 (n-1) to display 2n gradation.

[0077] In addition, in the example of drawing 11 , the display of 16 gradation is possible by 4-bit data. Moreover, with the configuration equipped with six sub-picture elements 50 as shown in drawing 13 , the display of 64 gradation is attained with 6-bit data. Of course, the electrode layout of a sub-picture element is not restricted to drawing 11 and drawing 13 .
[0078] Moreover, since it is not necessary to prepare the transistor of dedication for the dedicated line which supplies a blanking signal, or a blanking like the conventional example, the large numerical aperture of a pixel is taken and this invention can carry out the thing of it. And especially this invention concerning such a configuration is very effective in realizing the active-matrix mold EL display excellent in the homogeneity of a display, and gradation nature by adopting an area gradation method.
[0079] (Gestalt 4 of operation) It is characterized by driving the gestalt 4 of this operation by the operating condition to which the active region of the transistor Tr2 for a drive operates in a linear field in driving the indicating equipment of the gestalt of the above-mentioned implementation.
[0080] Since an EL element is a current control mold light emitting device from which brightness differs according to the current which flows a component, in order to lose display nonuniformity, it needs to carry out a constant current drive. As an approach of performing this constant current drive, there is a method of preparing a current regulator circuit in a pixel. However, with the configuration which prepares a current regulator circuit, the number of a transistor increases and the fall of the yield is caused. Then, even if the electrical potential difference impressed to the threshold of the transistor for a drive or the gate of the transistor for a drive varies, it can avoid almost affecting a current value by operating the transistor for a drive in a linear field with the gestalt 4 of this operation.
[0081] The result of having performed operating point analysis of EL element 11 and the transistor Tr2 (the P channel mold transistor was used) for a drive to drawing 14 is shown. In drawing 14 , Rhine L5 shows the electrical potential difference/current characteristic of EL element 11, and Rhine L6-L10 show the drain electrical potential difference / drain current characteristic of the transistor Tr2 for a drive. In addition, when Rhine L6 sets gate voltage to -1V, Rhine L7 sets gate voltage to -3V and Rhine L8 sets gate voltage to -4V, Rhine L9 is a drain electrical potential difference / drain current characteristic when Rhine L10 sets gate voltage to -6V, when gate voltage is set to -5V. Even when the gate voltage of a transistor changes so that clearly from drawing 14 , it is understood that the current value of the intersection of the drain electrical potential difference / drain current characteristic of the transistor Tr2 for a drive, and the electrical potential difference/current characteristic of EL element 11 is hardly influenced. Therefore, at the former, it can be used also with a transistor with a bad property which has been considered that it cannot bear use. Especially this is advantageous conditions when using polish recon as a transistor.
[0082] (Gestalt 5 of operation) Drawing 15 is the circuit diagram of EL display concerning the gestalt 5 of operation, and drawing 16 is a timing chart which shows luminescence actuation of EL display concerning the gestalt 5 of operation. The gestalt 5 of this operation is similar to the gestalt 1 of operation, and gives the same reference mark to a corresponding part. With the gestalt 1 of the above-mentioned implementation, although the blanking signal was supplied from the scanning line GL, exclusive wiring (wiring for blanking signals) which supplies a blanking signal is prepared, and it consists of gestalten 5 of this operation so that a blanking signal may be supplied from this wiring for blanking signals.
[0083] In addition, in drawing 15 , although only four pixels about signal-line SLm+1 of scanning-line GLn-1 of the n-1st line, the scanning line GLn of the n-th line and the signal line SLm of the m-th train, and the m+1st trains are drawn, it has the configuration with the same said of other pixels.
[0084] The configuration of the gestalt of this operation is explained with reference to drawing 15 . Wiring for blanking signals is prepared according to the individual for every line. In drawing 15 , BLn-1 is the n-th-1st-line wiring for blanking signals, and BLn is the n-th-line wiring for blanking signals. the object for blanking signals -- wiring BLn-1 is connected to one electrode of the auxiliary capacity 13 of each pixel belonging to the n-1st line. Moreover, the wiring BLn for blanking signals is connected to one electrode of the auxiliary capacity 13 of each pixel belonging to the n-th line. these objects for blanking signals -- wiring BLn-1 and BLn are connected common to the blanking signal drive circuit 80 -- having -- **** -- the blanking signal drive circuit 80 -- the object for blanking signals -- it is constituted so that the blanking signal of a predetermined electrical potential difference may be supplied to predetermined timing through wiring BLn-1 and BLn.
[0085] In addition, with the gestalt of this operation, since a blanking signal is not supplied from the scanning line GL, it replaces with the scanning-line side drive circuit 4, and the scanning-line side drive circuit (for example, scanning-line side drive circuit 4A of the gestalt 7 of operation mentioned later) which consists of a shift register and an output buffer is used.
[0086] Subsequently, with reference to drawing 16 , luminescence actuation of EL display of the above-mentioned configuration is explained. In addition, as shown in drawing 16 (a), a signal line SLm and the picture signal electrical potential difference Vs supplied to SLm+1 have two voltage levels, 7.4V and 12.4V, 7.4V shall show a luminescence condition and 12.4V shall show a nonluminescent condition. Moreover, the potential of the current supply source line 70 shall be set as 12.4V, and the potential of the cathode electrode of EL element 11 shall be set as 0V.
[0087] First, luminescence actuation of the pixel belonging to the n-1st line is explained. At time of day T1, the potential of scanning-line GLn-1 changes from high level (it is equivalent to V2 level and is 12.5V at the gestalt of this operation) to a low level (it is equivalent to V1 level and is 0V at the gestalt of this operation), as shown in drawing 16 (c). Thereby, the switching transistor Tr1 connected to scanning-line GLn-1 is turned on to the timing of this time of day T1, and a picture signal electrical potential difference (7.4V) is impressed to the gate electrode of

the transistor Tr2 for a drive through a signal line SLm and SLm+1. Here, the potential of the current supply source line 70 is 12.4V, and since the potential of the cathode electrode of EL element 11 is 0V, -5V are impressed between the gate sources of the transistor Tr2 for a drive. Therefore, the transistor Tr2 for a drive serves as ON, a current flows through EL element 11 from the current supply source line 70, and EL element 11 emits light. The auxiliary capacity 13 is connected to the gate electrode of the transistor Tr2 for a drive, and, thereby, gate voltage is held 7.4V.

[0088] Subsequently, the potential of blanking signal wiring BLn-1 can pull up to the timing of time-of-day T3 5V (it is equivalent to the blanking signal level V3) (it can pull up from the A point of drawing 16 (b) to a B point). On the other hand, the auxiliary capacity 13 is set as sufficiently big capacity value to the gate capacitance of the transistor Tr2 for a drive. Therefore, the potential of the gate electrode of the transistor Tr2 for a drive rises about [ 5 ] by V by the potential rise of blanking signal wiring BLn-1 of 5V. For this reason, the transistor Tr2 for a drive serves as OFF, and stops luminescence. This condition continues to the following write-in timing (time of day T5). Therefore, the period from time-of-day T3 to time of day T5 turns into a blanking period over the pixel of the n-1st line.

[0089] About the pixel of the n-th line, even time of day T6 serves as a blanking period from time-of-day T four similarly.

[0090] Of course, if needed, the timing which gives a blanking, and its time amount width of face can be given to arbitration so that effectiveness, such as the same period or a different period, may become max by adjusting the output timing of the blanking signal corresponding to each line.

[0091] Thus, a blanking signal can be impressed to the same period to all the pixels belonging to the same line, and it can shift during a sequential fixed period in each line, a blanking signal can be impressed, and more effective blanking actuation can be made to perform.

[0092] (Gestalt 6 of operation) Drawing 17 is the circuit diagram of the gestalt 6 of operation, and drawing 18 is the timing chart of luminescence actuation. The gestalt 6 of this operation is equipped with the blanking signal wiring BL like the gestalt 5 of the above-mentioned implementation, and is equivalent to the gestalt 5 of operation. [ of the fundamental actuation which makes EL element 11 emit light ] However, although it consisted of gestalten 5 of operation so that blanking signal wiring might drive independently to each line, with the gestalt 6 of this operation, the blanking signal wiring BL wired for every line has composition connected to the blanking signal drive circuit 80 through common Rhine 60. Therefore, the timing which gives a blanking signal will serve as the same period to all the pixels of the screen, if it puts in another way during this term to the pixel of all lines.

[0093] Below, luminescence actuation is explained with reference to drawing 18 . In the period from time of day T1 to time of day T2, sequential selection of the scanning lines GL1, GL2, --, GLn, --, the GLlast (the scanning line of a last line is meant) is made, and the pixel for every line carries out sequential luminescence. And the potential of the blanking signal wiring BL rises by 5V at the time of day 3 after selection of the pixel belonging to the scanning line GLlast was performed. Thereby, the pixel belonging to all lines stops luminescence by this time-of-day T3. That is, the whole screen serves as a black display by time-of-day T3. And by time-of-day T four, the potential of blanking signal wiring decreases by 5V, and will be in the condition of the original low level. Therefore, a blanking condition is canceled. That is, the period by time-of-day T3 - time of day 4 is equivalent to a blanking period. On the other hand, from this time-of-day T four, again, sequential selection of the scanning lines GL1, GL2, --, GLn, --, the GLlast is made, and the image of degree frame is displayed.

[0094] Thus, all pixels will be in a blanking condition to the same timing in the selection period of the last scanning line, and a blanking period will also become the same. Therefore, the gestalt 6 of this operation has the advantage in which the configuration of the blanking signal drive circuit 80 can be simplified compared with the gestalt 5 of operation.

[0095] However, in a period until the scanning line of the 1st line is chosen in the selection period of the last scanning line with the gestalt of this operation, since a blanking period is inserted, as compared with the gestalt 5 of operation, a blanking period is short. However, also in such a short period, it is checked by an invention-in-this-application person's etc. experiment that clear-ization of an image is obtained by insertion of a blanking period.

[0096] (Gestalt 7 of operation) Drawing 19 is the circuit diagram showing the configuration of the active-matrix mold EL display concerning the gestalt 7 of operation. The gestalt 7 of this operation is similar to the gestalt 1 of the above-mentioned implementation, gives the same reference mark to a corresponding part, and omits detailed explanation. Although the current supply source line 70 was formed, with the gestalt 7 of this operation, the current supply source line 70 is omitted, and it consists of gestalten 1 of the above-mentioned implementation so that a drive current may be supplied to EL element 11 from the scanning line GL. Moreover, the blanking signal is constituted so that it may be given to a direct EL element from the scanning line GL.

[0097] The configuration of EL display applied to the gestalt 7 of operation with reference to drawing 19 below is explained. In the gestalt 7 of this operation, the gate electrode of the transistor Tr1 for switching is connected to the scanning line GL, the source electrode of the transistor Tr1 for switching is connected to a signal line SL, it connects common to one electrode of the gate of the transistor Tr2 for a drive, and the auxiliary capacity 13, and the drain electrode of the transistor Tr1 for switching is constituted. Moreover, a source electrode is connected common to the electrode of another side of the preceding paragraph scanning line 3 which is the specific scanning line, and the auxiliary capacity 13, a drain electrode is connected to the anode electrode (it is equivalent to the pixel electrode 20) of EL element 11, and said transistor Tr2 for a drive is constituted.

[0098] Thus, while being able to omit a current supply source line and being able to aim at improvement in a

numerical aperture by considering as the configuration which supplies a drive current to EL element 11 with the preceding paragraph scanning line (equivalent to the specific scanning line), short generating between the signal lines and current supply source lines which were made into the problem in the former, or between the scanning line and a current supply source line can be prevented. In addition, the preceding paragraph scanning line and the path cord between EL elements 11 are not equivalent to an outgoing line from the preceding paragraph scanning line, and are not bus wiring like a current supply source line. Therefore, the above-mentioned path cord has very small line breadth compared with a current supply source line, therefore the area occupied to the pixel of a path cord is very small, and trouble is not caused to decline in a numerical aperture.

[0099] Moreover, with the gestalt 7 of this operation, it replaces with the scanning-line side drive circuit 4 of the gestalt 1 of operation, and scanning-line side drive circuit 4A is used. As shown in drawing 20 , this scanning-line side drive circuit 4A consists of a shift register 65 and an output buffer 40, and it is constituted so that the binary signal level of high level and a low level may be outputted alternatively.

[0100] Subsequently, the display action of the display of the above-mentioned configuration is explained. Drawing 21 is the timing chart of luminescence actuation of an EL element. Drawing 21 (a) is the wave form chart of a picture signal electrical potential difference, drawing 21 (b) is the wave form chart of the electrical potential difference of the scanning line GLa, and drawing 21 (c) is the wave form chart of the electrical potential difference of the scanning line GLb. In addition, two pixels 10a and 10b of explanation which is shown in drawing 22 for convenience and which adjoins up and down will be made into an example, and will be explained.

[0101] In addition, in drawing 22 , Subscript a is attached about the component relevant to pixel 10a (for example, the scanning line is a reference mark GLa and Tr1a etc. shows the transistor for switching), and Subscript b is attached about the component relevant to pixel 10b (for example, the scanning line is a reference mark GLb and Tr1b etc. shows the transistor for switching). Moreover, with the gestalt 7 of this operation, the cathode electrode potential (counterelectrode potential) of an EL element shall be set as 7.4V.

[0102] First, in the write-in period W1 (time of day T1 - time of day T2), as shown in drawing 21 (c), since the voltage level of the scanning line GLb is a low level (it is equivalent to V1 level and is 0V at the gestalt 7 of this operation), pixel 10b is chosen. And in this write-in period W1, a picture signal electrical potential difference (for example, 7.4V) is impressed to the gate of transistor Tr2b for a drive, and auxiliary capacity 13b through ** and the signal line SL with which transistor Tr1b for switching which is a P channel mold transistor is in ON condition. On the other hand, in the period of time of day T1-T2, since preceding paragraph pixel 10a is a non-selection period as shown in drawing 21 (b), the preceding paragraph scanning line GLa is high level (it is equivalent to V1 level and is 12.4V at the gestalt 7 of this operation), therefore 7.4-12.4=-5V are impressed between the gate sources of transistor Tr2b for a drive, and transistor Tr2b for a drive serves as ON. Thereby, through the preceding paragraph scanning line GLa and transistor Tr2b for a drive, a current flows towards a cathode electrode (counterelectrode) from the anode electrode (pixel electrode) of EL element 11b, and EL element 11b emits light. In addition, EL element 11a is emitting light by the above-mentioned luminescence actuation of EL element 11b, and same actuation.

[0103] Here, if it is the drive of a general EL element, as the imaginary line M of drawing 21 (b) shows, the preceding paragraph scanning line GLa will maintain high level to the write-in timing (time-of-day T four) of degree frame. However, in the gestalt 7 of this operation, as shown in drawing 21 (b), the preceding paragraph scanning line GLa changes from high level to a low level by former time-of-day T3 from time-of-day T four. Thereby, the potential (0V) of the preceding paragraph scanning line GLa becomes low rather than the cathode electrode potential (7.4V) of EL element 11b. Therefore, the current supply source to EL element 11b stops, and EL element 11b stops luminescence. Namely, pixel 10b will be in a blanking condition by time-of-day T3. And the preceding paragraph scanning line GLa is still a low level until the write-in period W1 (time-of-day T-four-T5) of preceding paragraph pixel 10a is completed. Therefore, EL element 11b is still a blanking condition.

[0104] In addition, in the preceding paragraph scanning line GLa, the period of a low level to time-of-day T3 - T four is a period when the blanking signal V3 for carrying out the blanking of the pixel 10b is outputted, and the period of a low level to time-of-day T-four-T5 is the write-in period W1 for writing a picture signal in pixel 10a. However, in the gestalt of this operation, since the blanking signal level is set as the value which was in agreement with the low level (0V) of a scan signal, as shown in drawing 21 (b), all the periods to time-of-day T3-T5 are the periods of a low level.

[0105] Subsequently, the potential of the preceding paragraph scanning line GLa changes from a low level high-level at time of day T5. Therefore, according to the potential written in the gate electrode of transistor Tr2a for a drive in the write-in period, the current of the preceding paragraph scanning line GLa further supplied from the preceding paragraph scanning line (not shown) is controlled, and light is flowed and emitted to EL element 11a. Here, since the picture signal electrical potential difference of a write-in period (period of time-of-day T-four-T5) is 12.4V, EL element 11a has stopped luminescence. Of course, if a picture signal electrical potential difference is 7.4V, EL element 11a will emit light.

[0106] Moreover, EL element 11b will also be in a luminescence condition or a luminescence idle state according to the picture signal electrical potential difference written in the gate electrode of transistor Tr2a for a drive by the same actuation as the above-mentioned EL element 11a.

[0107] In the above-mentioned example, although the blanking signal level V3 was set up identically to the low level (0V) of a scan signal, it is not limited to this. That is, if the blanking signal level V3 is smaller than the potential of the cathode electrode (counterelectrode) of an EL element, it is enough and, thereby, can stop the current to an EL

element. However, in this case, since the potential of the scanning line GL needs three electrical-potential-difference level signals V1-V3, as a scanning-line side drive circuit, it is replaced with scanning-line side drive circuit 4A, and the scanning-line side drive circuit 4 of the gestalt 1 of operation should just be used for it.
[0108] Moreover, since the preceding paragraph scanning line GLa is a low level in the blanking period of EL element 11b, even if transistor Tr1a for switching is in ON condition and 7.4V are written in transistor Tr2a for a drive in the period, it will be in the blanking condition of EL element 11a. Because, before being in the blanking condition of EL element 11b, EL element 11a is in the blanking condition. Therefore, it is because the potential of the scanning line (further scanning line [ Preceding paragraph scanning line GLa ] of the preceding paragraph) which supplies a current to EL element 11a serves as a low level even if 7.4V are written in transistor Tr2a for a drive, so a current is not supplied to EL element 11a but luminescence has stopped uninfluential in the potential of the gate electrode of transistor Tr2a for a drive.
[0109] Also although the above-mentioned example is explained and excels about luminescence about Pixels 10a and 10b and blanking actuation which adjoin up and down, luminescence and blanking actuation are performed by actuation with the same said of other pixels.
[0110] Thus, with the gestalt 7 of this operation, while the scanning line serves as a current supply source line, a blanking signal can be outputted from the scanning line.
[0111] In addition, although the transistor Tr2 for a drive can also use an N channel mold transistor if it states to reference, it is desirable to use a P channel mold transistor like the gestalt of this operation. It is because an electrical potential difference required for an electrical potential difference with the gate voltage higher than the anode of an EL element for making the transistor Tr2 for a drive into ON condition to be needed, and drive a active-matrix mold EL element will increase if the transistor Tr2 for a drive is formed with an N channel mold transistor.
[0112] (Gestalt 8 of operation) Drawing 23 is the circuit diagram of EL display concerning the gestalt 8 of operation, and drawing 24 is the timing chart of luminescence actuation of EL display concerning the gestalt 8 of operation. In addition, drawing 24 (a) is the wave form chart of a picture signal electrical potential difference, drawing 24 (b) is the wave form chart of the electrical potential difference of the scanning line GLc, and drawing 24 (c) is the wave form chart of the electrical potential difference of the scanning line GLd. The gestalt 8 of this operation gives the same reference mark to the part which is similar and corresponds to the gestalt 7 of operation. With the gestalt 8 of operation, the transistor for switching and the transistor for control are N channel mold transistors. Moreover, the anode electrode of an EL element is used as a counterelectrode, and a cathode electrode is used as a pixel electrode, and it is constituted by the current which flows towards the scanning line from an EL element so that an EL element may emit light.
[0113] Two pixels 10c and 10d which are shown below at drawing 23 and which adjoin up and down are made into an example, and luminescence and blanking actuation of the gestalt of this operation will be explained. In addition, with the gestalt 8 of this operation, anode electrode potential (counterelectrode potential) shall be set as 3.0V.
[0114] First, in the write-in period W1 (from time of day T1 to time of day T2) of 10d of pixels, as shown in drawing 24 (c), since the voltage level of the scanning line GLd is high level (it is equivalent to V1 level and is 12.4V at the gestalt 8 of this operation), 10d of pixels is chosen. And in this write-in period W1, since transistor Tr1d for switching which is an N channel mold transistor is in ON condition, it is impressed to the gate whose picture signal electrical potential difference (for example, 5.0V) is transistor Tr2d for a drive, and the auxiliary capacity of 13d through a signal line SL. Since preceding paragraph pixel 10c is a non-selection period on the other hand as the period of this time of day T1-T2 shows to drawing 24 (b), Since the preceding paragraph scanning line GLc is a low level (it is equivalent to V2 level and is 0V at the gestalt 8 of this operation) and anode electrode potential (counterelectrode potential) is set as 3.0V, 5.0-3.0=2V are impressed between the gate sources of transistor Tr2d for a drive, and transistor Tr2d for a drive serves as ON. Thereby, a current flows towards the preceding paragraph scanning line GLc from 11d of EL elements, and 11d of EL elements emits light.
[0115] Here, if it is the drive of a general EL element, as the imaginary line M of drawing 24 (b) shows, the preceding paragraph scanning line GLc will maintain a low level to the write-in timing (time-of-day T four) of degree frame. However, in the gestalt 7 of this operation, as shown in drawing 24 (b), the preceding paragraph scanning line GLc changes from a low level (the gestalt of this operation 0 V) high-level by former time-of-day T3 from time-of-day T four. Thereby, the potential (12.4V) of the preceding paragraph scanning line GLc becomes high rather than the anode electrode potential (3.0V) of 11d of EL elements. Therefore, the current supply source of 11d of EL elements stops, and 11d of EL elements stops luminescence. Namely, 10d of pixels will be in a blanking condition by time-of-day T3. And the preceding paragraph scanning line GLc is still high-level until the write-in period W1 (time-of-day T-four-T5) of preceding paragraph pixel 10c is completed. Therefore, 11d of EL elements is still a blanking condition. Thus, while 11d of EL elements emits light in an one-frame period according to a picture signal, the BURANKIN condition which luminescence stops will be acquired. The luminescence as 11d of EL elements also with the same EL element and blanking actuation of the remainders other than 11d of EL elements are performed.
[0116] Thus, also in the gestalt of this operation, a blanking period can be inserted into one frame.
[0117] In addition, in the preceding paragraph scanning line GLc, the high-level period to time-of-day T3 - T four is a period when the blanking signal V3 for carrying out the blanking of the 10d of the pixels is outputted, and the high-level period to time-of-day T-four-T5 is the write-in period W1 in order to write a picture signal in pixel 10c. However, in the gestalt of this operation, since the blanking signal level is set as the value which was in agreement with the high level (12.4V) of a scan signal, as shown in drawing 24 (b), all the periods by time of day T1-T5 are the periods of a low level.

[0118] In the above-mentioned example, although the blanking signal level V3 was set up identically to the high level (12.4V) of a scan signal, it is not limited to this. That is, if the blanking signal level V3 is higher than the potential of the anode electrode (counterelectrode) of an EL element, it is enough and, thereby, can stop the current to an EL element.
[0119] (Gestalt 9 of operation) The gestalt 9 of operation is characterized by the sum of the output impedance of the last stage buffer in scanning-line side drive circuit 4A connected to the impedance of the specific scanning line GL and this specific scanning line GL considering as 20% or less to the impedance of the EL element by which parallel connection is carried out to this specific scanning line GL in the configuration of the gestalt 7 of operation. And by regulation of such an impedance, sufficient electrical potential difference for an EL element can be impressed, and a uniform display can be realized. Hereafter, with reference to drawing 25 and drawing 26 , why a uniform display is realizable with regulation of an impedance is explained.
[0120] Drawing 25 is an equal circuit including the EL element which drives the scanning line and this scanning line in case the pixel electrode connected to the transistor for a drive turns into an anode electrode according to the flowing current, and drawing 26 shows an equal circuit including the EL element which drives the scanning line and this scanning line in case the pixel electrode connected to the transistor for a drive turns into a cathode electrode according to the flowing current. In drawing 25 and drawing 26 , 40 shows the buffer of the last stage of scanning-line side drive circuit 4A, 41 shows resistance of the scanning line GL, and 42 shows the capacity of the scanning line GL. As shown in drawing 25 , when the anode electrode of EL element 11 turns into a pixel electrode, a current flows to EL element 11 through the output impedance of a buffer 40, and the impedance of the scanning line GL. As shown in drawing 26 , when the cathode electrode of EL element 11 turns into a pixel electrode, a current flows towards the scanning line GL from EL element 11. Even if it is which type of drawing 25 and drawing 26 , if the output impedance of a buffer 40 and the impedance of the scanning line GL are high as compared with the impedance of EL element 11, when a current flows, a voltage drop will arise with the scanning line etc., and sufficient electrical potential difference will not be impressed to EL element 11.
[0121] The result of having performed circuit simulation to this equal circuit is shown in drawing 27 . In drawing 27 , Rhine L1 shows the input of a buffer 40, and Rhine L2 shows the output of a buffer 40. Rhine L3 shows the potential of the last train edge K (refer to drawing 25 and drawing 26 ) in case the sum of the impedance of the scanning line GL and the output impedance of a buffer 40 is about 2% of the impedance of the scanning line. Rhine L4 shows the potential of the last train edge K in case the sum of the impedance of the scanning line GL and the output impedance of a buffer 40 is 20% of the impedance of the scanning line GL. If the sum of an output impedance and the impedance of the scanning line GL exceeds 20% to the impedance of EL element 11 of each pixel so that more clearly than drawing 27 , it will be admitted that the potential of the last train edge K of the scanning line GL falls greatly. Therefore, sufficient electrical potential difference for EL element 11 is no longer impressed, and a uniform display is not obtained.
[0122] In addition, in order to reduce the output impedance of scanning-line side drive circuit 4A, you may make it prepare voltage HOROA in the last stage of for example, a scanning-line side drive circuit.
[0123] (Gestalt 10 of operation) Drawing 28 is the top view of the display of the display concerning the gestalt 10 of operation, and drawing 29 is the circuit diagram. In addition, drawing 28 and drawing 29 show only the configuration about 1 pixel. The gestalt 10 of this operation divides one unit pixel in the gestalt 7 of operation into two or more fields, and is characterized by indicating by gradation with an area gradient method. Hereafter, a concrete configuration is explained with reference to drawing 28 and drawing 29 . The unit pixel 10 has the structure divided into two or more fields (the gestalt 4 of this operation four). The configuration of the sub-picture element 50 which is this division field is the same as the configuration of the unit pixel 10 in the gestalt 1 of the above-mentioned implementation. That is, a sub-picture element 50 has the transistor Tr1 for switching, the transistor Tr2 for a drive, and the auxiliary capacity 13 while having the scanning line GL, respectively. As for the source of the transistor Tr1 for a drive, it is desirable to consider as the configuration connected to the scanning line of the adjoining sub-picture element. It realizes by combining luminescence/nonluminescent one of the divided sub-picture element field as the method of presentation of gradation. In addition, a digital picture signal is supplied to a signal line SL.
[0124] As the concrete approach of a gradation display, weighting of the area for a light-emitting part of EL element 11 in the sub-picture element 50 divided into two or more fields is carried out corresponding to the bit. Thus, it does not divide into division into equal parts, but the surface ratio for a light-emitting part is corresponded to a bit, and it is 1:2:4. : -- It becomes possible by carrying out weighting to :2 (n-1) to display 2n gradation.
[0125] In addition, in the example of drawing 28 , the display of 16 gradation is possible by 4-bit data. Moreover, with the configuration equipped with six sub-picture elements 50 as shown in drawing 30 , the display of 64 gradation is attained with 6-bit data. Of course, the electrode layout of a sub-picture element was not restricted to drawing 28 and drawing 30 .
[0126] Thus, it is very effective in realizing the active-matrix mold EL display excellent in the homogeneity of a display, and gradation nature by there being no current supply source line of dedication, and adopting an area gradation method especially in this invention which is the configuration which can take the large numerical aperture which is a pixel.
[0127] (Gestalt 11 of operation) Drawing 31 is the circuit diagram of the active-matrix mold EL display concerning the gestalt 11 of operation. The gestalt 11 of this operation is similar to the gestalt 7 of operation, and gives the same reference mark to a corresponding part. In addition, drawing 31 shows only the configuration about a unit pixel. With the gestalt 11 of this operation, it has the transistor Tr4 for switching ON/OFF control is carried out [ the

transistor ] by the transistor Tr3 for switching and transistor reset signal by which are characterized by considering as the circuitry which has an offset canceller function, and ON/OFF control is carried out with the current switch signal other than the transistor Tr1 for switching, and the transistor Tr2 for a drive.
[0128] Subsequently, explanation of the offset canceller function in the above-mentioned circuit carries out memory of the threshold electrical potential difference Vt of a transistor Tr2 to a capacitor C1 first. In the period whose transistor Tr1 is OFF, a transistor Tr3 is OFF and, specifically, a transistor Tr4 is set to ON. Thereby, the electrical potential difference between terminals of a capacitor C1 rises to Vt. That is, it means that memory of the Vt was carried out to the capacitor C1. If potential of the scanning line GL is set to Vdd at this time, the potential of a node 71 will serve as Vdd-Vt.
[0129] Subsequently, a transistor Tr3 is ON, and a transistor Tr4 is set to OFF, and an EL element and the scanning line GL (equivalent to a current supply source line) will be in a connection condition.
[0130] Subsequently, a transistor Tr3 is ON, and a transistor Tr1 serves as ON in the state of OFF of a transistor Tr4, and the picture signal electrical potential difference Von is impressed to the gate of a transistor Tr2 through a capacitor C2. Since memory of the Vt is beforehand carried out to the capacitor C1 at this time, the potential (equivalent to the gate potential of a transistor Tr2) of a node 71 serves as Von+Vdd+Vt. Therefore, since the current value of a transistor Tr2 is set to f (Von+Vdd+Vt-Vt) and it becomes the function about a value with which Vt was offset, even if variation is in the threshold Vt of a transistor Tr2, an EL element can be driven, without being influenced by it.
[0131] And in the configuration which has the above-mentioned offset canceller function, by connecting the scanning line GL to the source of the transistor Tr2 for a drive, a current can be supplied to EL element 11 from the scanning line GL like the gestalt of the above-mentioned implementation, and a blanking signal can be given from the scanning line GL in the gestalt of this operation.
[0132] (Other matters)
(1) With the gestalten 1-4 of the above-mentioned implementation, although the gate of the transistor for a drive is connected with the latter-part scanning line through auxiliary capacity and the blanking signal was given from the latter-part scanning line, this invention is not limited to this. That is, it replaces with the latter-part scanning line, which the scanning line is connected with auxiliary capacity, and you may make it give a blanking signal from the scanning line. It is also possible to follow, for example, to use the own scanning line of a selection pixel. However, in this case, with the change to the OFF from ON of a selection pulse, it is the effect of the parasitic capacitance of the transistor for a drive connected to the own scanning line of a pixel, it is expected that the potential of a pixel electrode changes, and in order to prevent this, it is necessary to add big storage capacitance. It is possible to solve this problem by making into the latter-part scanning line the scanning line which gives a blanking signal about this point. Because, by making into the latter-part scanning line the scanning line which gives a blanking signal, leading about of wiring also has a merit, such as becoming it being good at necessary minimum and possible to also suppress the potential fluctuation by the parasitic capacitance of a transistor to the minimum. Therefore, as for the specific scanning line, it is desirable to consider as the latter-part scanning line of a pixel.
[0133] (2) the transistor Tr1 for switching in the gestalten 1-11 of the above-mentioned implementation has little leakage current as the property demanded -- in other words, what has the good maintenance property of data is desired. Therefore, as for the transistor Tr1 for switching, it is desirable to use the thing of the multi-gate structure where two or more transistors were connected to the serial, or LDD (Lightly doped drain) structure, and if it does in this way, it can acquire a good OFF property.
[0134] (3) The transistors Tr1 and Tr2 in the gestalten 1-11 of the above-mentioned implementation may be formed with an amorphous silicon, and you may make it form them by polish recon. However, when forming by polish recon, polish recon has large mobility as compared with an amorphous silicon, and since detailed-izing of a component is easy, it is advantageous especially when using two or more transistors into 1 pixel like this invention.
[0135] (4) You may make it really form either [ at least ] a scanning-line side drive circuit or a signal-line side drive circuit on a glass substrate in the gestalten 1-11 of the above-mentioned implementation, when producing a transistor by low-temperature polish recon at the same time it produces the transistor of a picture element part. Thus, by making a circumference drive circuit into a built-in drive circuit, power consumption can be reduced sharply and light weight and thin shape-ization of the whole display can be attained.
[0136] (5) In driving the indicating equipment of the gestalten 7-11 of operation, you may make it drive like the gestalt 4 of operation by the operating condition to which the active region of the transistor Tr2 for a drive operates in a linear field.
[0137] (6) Although the specific scanning line was made into the preceding paragraph scanning line to the scanning line connected to a selection pixel with the gestalten 7-11 of operation, it is [ that this invention is not limited to this and should just be which the scanning line ] also possible to use the own scanning line of a selection pixel. However, in this case, with the change to the OFF from ON of a selection pulse, it is the effect of the parasitic capacitance of the transistor for a drive connected to the own scanning line of a pixel, it is expected that the potential of a pixel electrode changes, and in order to prevent this, it is necessary to add big storage capacitance. It is possible by making the specific scanning line into the scanning line of the preceding paragraph about this point to solve this problem. It is because the potential of the gate electrode of the transistor for a drive is uniformly held from the time of write-in termination to write-in initiation of the pixel of the preceding paragraph in the following frame. And leading about of wiring also has a merit, such as becoming it being good at necessary minimum and possible to also suppress the potential fluctuation by the parasitic capacitance of a transistor to the minimum, by

making the specific scanning line into the scanning line of the preceding paragraph. Therefore, as for the specific scanning line, it is desirable to consider as the preceding paragraph scanning line of a pixel.
[0138] (7) This invention may be the configuration which is not limited to the gestalten 1-11 of operation, chose the gestalten 1-11 of operation suitably, and combined them.
[0139]
[Effect of the Invention] According to the configuration of this invention, the following effectiveness is done so as mentioned above.
(1) The EL element of each pixel emits light according to a picture signal, and while the image to wish to have is displayed, the blanking period when an EL element does not emit light will be inserted into one frame. Therefore, in a movie display, a black display is inserted between the images of a frame last time the image of a frame, and next time. Consequently, an after-image phenomenon can be controlled and a clear image can be recognized now.
[0140] (2) Moreover, the transistor of dedication for a blanking and wiring for blanking signals become unnecessary by supplying a blanking signal through the scanning line. Therefore, the numerical aperture of the part improves.
[0141] (3) Moreover, the current supply source line of the dedication for supplying a current to an EL element becomes unnecessary by supplying a current to an EL element from the specific scanning line. Consequently, while being able to make a numerical aperture larger than the conventional example, generating of the line defect short depended in the short-circuit between layers resulting from a current supply source line and a layer can be prevented, and EL display whose yield improved can be constituted.

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[Translation done.]